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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,814	11/21/2003	Naoyuki Kamei	60341 (70904)	3310

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EXAMINER	
RUTZ, JARED IAN	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,814	KAMEI ET AL.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12072005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 as originally filed on 11/21/2003 are pending in the instant application. Of these, there are 3 independent claims and 15 dependent claims.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 11/21/2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-18** are rejected under 35 U.S.C. 102(b) as being anticipated by Ramsey et al (US 5,813,022).

6. **Claim 1**

a. *A CPU, comprising: a cache.* Column 5 lines 19-23 shows the use of a Pentium P54 processor, which inherently contains a cache as shown by the article Intel Pentium ("P5"/"P54C") found at http://www.tvdsb.on.ca/banting/cicp/hardware/pcguide/ref/cpu/fam/g5-P54.html.

b. *And control means.* Figure 2 item 210 shows a cache memory controller, discussed at column 5 lines 39-51.

c. *Wherein data are written into the cache and write back is performed to reflect the data written into the cache to an external memory at a desired timing.* Page 4 of the article Intel Pentium ("P5"/"P54C") shows that the P54 uses write-back as a cache write policy. In a write-back cache management policy data is not immediately written back to main memory, but is held modified in the cache until it is necessary to be written to main memory, which is a desired timing.

d. *The control means determining whether or not processing of a task is possible only with access to the cache in accordance with the amount of memory needed to process the task, and then, when it is determined that the processing is possible, inhibiting access to the external memory.* This is the standard behavior for a cache. If the data needed is held in the cache, the copy of the data held in the cache is used and external memory is not accessed. If the cache does not hold the needed data, processing of the task is not possible only with access to the cache. See the definition of cache in the Microsoft Computer Dictionary.

7. Claim 2

e. The CPU according to claim 1, wherein: the control means detect free space in the cache and/or the amount of memory needed to process a task. It is inherent that the control means detects the amount of free space in the cache. A cache controller handles the residency of data in the cache, and in order to move data into the cache the controller must be aware of the free space in the cache.

8. Claim 3

f. The CPU according to claim 2, wherein: in a situation where access to the external memory is inhibited, when the control means determine that the processing is impossible only with access to the cache, or when a cache miss occurs, the control means permit access to the external memory. See the definition of cache in the Microsoft Computer Dictionary, which shows that when needed data is not held in the cache main memory is accessed.

9. Claim 4

g. The CPU according to claim 1, further comprising: clock control means for controlling a clock frequency of an internal clock, the clock control means changing the clock frequency when access to the external memory is inhibited. See column 9 lines 3-5, which show that the clock signal input to the processor may be slowed to place the microprocessor in the stop grant state. The microprocessor enters a stop grant state when signal STPCLK* is asserted

(column 9 lines 1-3). STPCLK* is asserted by miscellaneous logic chip 132. When the microprocessor is in stop grant state access to the external memory is inhibited.

10. Claim 5

h. The CPU according to claim 1, wherein: the control means detect an address of a location where unnecessary data are stored in the cache and then free a cache space corresponding to the detected address. This is inherently performed by the cache controller. When an address in a cache contains data that is determined to no longer be according to the cache replacement policy, that location can be used to hold a new data value.

11. Claim 6

i. The CPU according to claim 1, wherein: at an initial stage after power-on of the CPU, access to the external memory is inhibited after a program and data are loaded into the cache from the external memory. The stop grant state would occur after the power-on of the processor. Lines 7-9 of the Abstract show that the stop grant state is entered after the system has been idle for a predetermined period of time. As the processor is executing instructions before becoming idle, programs and data have been loaded into the cache before the system enters a stop grant state.

12. Claim 7

j. The CPU according to claim 1, wherein: the control means determine whether or not access to the external memory is needed when a state of a task changes. The entry for cache in the Microsoft Computer Dictionary explains that when a processor references an address in memory (which is a change of state, as data not held in the processor registers is needed), the cache checks to see whether it holds that address. If it does hold that address, the data is returned to the processor; if it does not, a regular memory access occurs.

13. Claim 8

k. The CPU according to claim 1, wherein: the control means determine whether or not a program and data in the cache are purged, and then, if not purged, avoid loading the program and the data into the cache from the external memory. If data has not been purged from the cache, it is present in the cache. Accordingly, as taught by the Microsoft Computer Dictionary, any requests for that data will be retrieved from the cache and not retrieved from main memory.

14. Claim 9

l. An information processing device comprising: a CPU which writes data into a cache provided therein and performs write back to reflect the written data into the cache to an external memory at a desired timing the external memory.

Page 4 of the article Intel Pentium ("P5"/"P54C") shows that the P54 uses write-back as a cache write policy.

m. And power supplying means for supplying power to the external memory. It is inherent that the computer system shown in figure 1 has a power supply, and that the external memory receives power.

n. The CPU including control means for determining whether or not processing of a task is possible only with access to the cache in accordance with the amount of memory needed to process the task, and then, when it is determined that the processing is possible, inhibiting access to the external memory. This is the standard behavior for a cache. If the data needed is held in the cache, the copy of the data held in the cache is used and external memory is not accessed. If the cache does not hold the needed data, processing of the task is not possible only with access to the cache. See the definition of cache in the Microsoft Computer Dictionary.

o. The power supplying means stopping power supply to the external memory when access to the external memory is inhibited. See column 7 lines 58-61, which show that the external L2 cache memory (item 208 of figure 2) are put in low power state when the processor enters a stop grant state

15. Claim 10

p. The information processing device according to claim 9, the external memory includes a plurality of modules. Column 6 lines 10-11 teach the use of two banks of memory in the L2 cache.

q. And the control means control power supply with respect to each of the modules. Column 8 lines 38-40 show that the banks of cache memory are put into low power mode by deasserting their chip select inputs. This shows that the power is controlled with respect to each bank of the cache memory.

16. Claim 11

r. A controlling method of a CPU which writes data into a cache included therein and performs write back to reflect the data written into the cache to an external memory at a desired timing. Page 4 of the article Intel Pentium ("P5"/"P54C") shows that the P54 uses write-back as a cache write policy

s. The method comprising the steps of: determining whether or not processing of a task is possible only with access to the cache in accordance with the amount of memory needed to process the task. As shown by the Microsoft Computer Dictionary, a cache determines if processing of a task is possible only with access to the cache by determining if requested data is held in the cache.

t. And when it is determined that the processing is possible, inhibiting access to the external memory. As shown by the Microsoft Computer Dictionary, if requested data is in the cache (processing is possible only with access to the cache), external memory is not accessed.

17. Claim 12

u. The method according to claim 11, further comprising the step of: detecting free space in the cache and/or the amount of memory needed to process a task. It is inherent that the control means detects the amount of free space in the cache. A cache controller handles the residency of data in the cache, and in order to move data into the cache the controller must be aware of the free space in the cache.

18. Claim 13

v. The method according to claim 12, further comprising the step of: in a situation where access to the external memory is inhibited, when it is determined that the processing is impossible only with access to the cache, or when a cache miss occurs, permitting access to the external memory. As shown by the Microsoft Computer Dictionary, if requested data is not held in the cache a request is made for the data to an external memory.

19. Claim 14

w. The method according to claim 11, further comprising the step of: when access to the external memory is inhibited, changing a clock frequency of an internal clock. See column 9 lines 3-5, which show that the clock signal input to the processor may be slowed to place the microprocessor in the stop grant state.

The microprocessor enters a stop grant state when signal STPCLK* is asserted (column 9 lines 1-3). STPCLK* is asserted by miscellaneous logic chip 132. When the microprocessor is in stop grant state access to the external memory is inhibited.

20. Claim 15

x. The method according to claim 11, further comprising the steps of: detecting an address of a location where unnecessary data are stored in the cache; and freeing a cache space corresponding to the detected address. This is inherently performed by the cache controller. When an address in a cache contains data that is determined to no longer be according to the cache replacement policy, that location can be used to hold a new data value.

21. Claim 16

y. The method according to claim 11, further comprising the step of: at an initial stage after power-on of the CPU, inhibiting access to the external memory after a program and data are loaded into the cache from the external memory. The stop grant state would occur after the power-on of the processor. Lines 7-9 of the Abstract show that the stop grant state is entered after the system has been idle for a predetermined period of time. As the processor is executing instructions before becoming idle, programs and data have been loaded into the cache before the system enters a stop grant state.

22. Claim 17

z. The method according to claim 11, further comprising the step of: determining whether or not access to the external memory is needed when a state of a task changes. The entry for cache in the Microsoft Computer Dictionary explains that when a processor references an address in memory (which is a change of state, as data not held in the processor registers is needed), the cache checks to see whether it holds that address. If it does hold that address, the data is returned to the processor; if it does not, a regular memory access occurs.

23. Claim 18

aa. The method according to claim 11, further comprising the steps of: determining whether or not a program and data in the cache are purged; and if not purged, avoiding loading the program and the data into the cache from the external memory. If data has not been purged from the cache, it is present in the cache. Accordingly, as taught by the Microsoft Computer Dictionary, any requests for that data will be retrieved from the cache and not retrieved from main memory.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jared I Rutz
Examiner
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jir

DONALD SPARKS
SUPERVISORY PATENT EXAMINER